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10/804,712	03/18/2004	Rafael Camarota	015114-069900US	7512

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,712	CAMAROTA ET AL.	
	Examiner	Art Unit	
	QUAN TRA	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,23-32,34 and 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,23-32,34 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 3/25/08. New rejections are introduced as necessitated by amendment.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-16, 23-26, 32, 34 and 35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The original specification fails to teach that the resistor and circuit, which is referred as “a second integrated circuit chip” in the claims, that drives the resistor are on separate chips.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyanaga et al. (USP 5514893) in view of Verhaege et al. (USP 6529359) and Djakovic (USP 6351539).

As to claim 1, Miyanaga et al.'s figure 1 shows a electronic system comprising: a first integrated circuit comprising: an input buffer (6, 7) coupled between a first supply terminal and a second supply terminal and having an input directly connected to a pad (1); and a clamp diode (2) coupled between the pad and the first supply terminal. Thus, figure 1 shows all elements of the claim except for a detail of a driver circuit, not shown, that providing driving signal to pad 1. However, Verhaege et al.'s figure 1 shows a driver circuit with ESD protection. Therefore, it would have been obvious to one having ordinary skill in the art to use Verhaege et al.'s driver circuit to drive Miyanage et al.'s circuit figure 1 for the purpose of protecting Miyanaga's circuit and the driver itself, thereby saving cost by preventing parts replacement. Thus, the modified Miyanaga et al.'s figure 1 further shows a resistor (Verhaege et al.'s Rout) having a first terminal coupled to the pad, and a second terminal coupled to receive an input signal; a second integrated circuit (Verhaege et al.'s 20, 22, 30, 38, 44, 34) coupled to the second terminal of the resistor to provide the input signal, wherein the resistor is not on the first integrated circuit or the second integrated circuit. The modified Miyanaga et al.'s figure 1 further fails to show that the circuit figure 1 and the added circuit are on separate chips (the resistor is not the first integrated circuit chip). However, Diakovic teaches in col. 6, lines 13-18, that making circuits on separate chips has the advantage that it provides separate access for each of the module, and if one of the blocks becomes compromised it can be replaced without affecting the others. Therefore, it would have been obvious to one having ordinary skill in the art to make Miyanaga et al.'s circuit figure 1 and the added driver on separate chips for the purpose of providing separate access for each circuit.

As to claim 3, Miyanaga et al.'s figure 1 shows that the clamp diode has an anode and a cathode, the anode is coupled to the pad and the cathode is coupled to the first supply terminal.

As to claim 4, Miyanaga et al.'s figure 1 shows that the first supply terminal receives a positive supply voltage, and the second supply voltage receives a ground supply.

As to claim 5, Miyanaga et al.'s figure 1 shows a pull-up output device (4) coupled between the first supply terminal and the pad; and a pull-down output device coupled between the pad and the second supply voltage terminal.

As to claim 6, Miyanaga et al.'s figure 1 shows that the pull-up device has a gate coupled to a first predriver circuit (8), and the pull-down device hag a gate coupled to a second predriver circuit (9).

As to claim 7, the modified Miyanaga et al.'s figure 1 fails to show logic gate coupled to drive the predriver. However, it is notoriously well known in the art buffer circuit, such as inverter, is for isolating and shaping signal. Therefore, it would have been obvious to one having ordinary skill in the art to use buffer circuit, such as inverter, to driver the predirvers 8 and 9 for the purpose of buffering their inputs signals.

3. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyanaga et al. (USP 5514893) in view of Verhaege et al. (USP 6529359), Djakovic (USP 6351539) and Toyashima (US 20010017755).

The modified Miyanaga et a1.'s figure 1 shows all limitations of the claim except for a switch coupled between the pad and the clamp diode. However, Toyashima's figure 2 shows a circuit having switch F1 coupled between pad 10 and clamp diode D1 to remove the clamp circuit when circuit operates at high speed. Therefore, it would have been obvious to one having ordinary skill in the art to add switches between Miyanaga et al.'s input pad and the diodes for the purpose of capable of increasing the circuit speed.

4. Claims 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyanaga et al. (USP 5514893) in view of Verhaege et al. (USP 6529359), Djakovic (USP 6351539) and Kwon et al. (US 20020163768).

As to claim 9, the modified Miyanaga et al.'s figure 1 shows all limitations of the claim except for a series of clamp diodes coupled between the pad and the second supply terminal. However, Kwon's figure 4 shows a plurality of clamp diodes (D41-D4n) coupled between pad 210 and second power supply Vss. Therefore, it would have been obvious to one having ordinary skill in the art to employ Kwon's teaching by adding plurality of clamp diodes (D41-D4n) connected between Miyanaga's pad and the second power supply for the purpose of further protecting the internal circuit.

As to claim 10, the modified Miyanaga et al.'s figure 1 shows that the series of clamp diodes comprises four diodes.

As to claim 11, the modified Miyanaga et al.' s figure 1 a pull-up output device (4) coupled between the first supply terminal and the pad. Figure 1 fails to show that the well terminal of the pull-up device is coupled to the first supply terminal. However, transistor with well connected to its source is well known in the art, i.e. figure 1 of the cited USP 6525594, for reducing leakage current. Therefore, it would have been obvious to one having ordinary skill in the art connected the well of Miyanaga's transistor 4 to its source or Vdd for the purpose of reducing leakage current.

As to claim 12, the modified Miyanaga et al.' s figure 1 shows that each of the clamp diodes in the series of clamp diodes has an anode and a cathode, the anode of one of the clamp diodes in the series of clamp diodes is coupled to the pad, and the cathode of one of the clnmp diodes in the series of clamp diodes is coupled to the second supply terminal.

As to claim 13, Miyanaga et al.' s figure 1 shows that the first supply terminal receives a positive supply voltage, and the second supply voltage receives a ground supply.

As to claim 14, Miyanaga et al.' s figure 1 shows that the integrated circuit further comprises a pull-up output device (4) coupled between the first supply terminal and the pad; and a pull-down output device (5) coupled between the pad and the second supply terminal.

As to claim 15, Miyanaga et al.' s figure 1 shows that the pull-up device has a gate coupled to a first predriver circuit (8), and the pull-down device has a gate coupled to a second predriver circuit (9).

As to claim 16, the modified Miyanaga et al.'s figure 1 fails to show logic gate coupled to drive the predriver. However, it is notoriously well known in the art buffer circuit, such as inverter, is for isolating and shaping signal. Therefore, it would have been obvious to one having ordinary skill in the art to use buffer circuit, such as inverter, to driver the predirvers 8 and 9 for the purpose of buffering their inputs signals.

5. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyanaga et al. (USP 5514893) in view of Verhaege et al. (USP 6529359), Djakovic (USP 6351539), Toyashima (US 20010017755) and Sher (USP 6417721).

The modified Miyanaga et al.'s figure 1 shows all elements of the claims except for the switch is a transistor (see the rejection of claim 8). However, Sher's figures 2A-2F shows that transistor and fuse are type of switches. One skill in the art would have recognized that fuse is not re-closed if opened, and transistor's state is reversible if opened/closed. Therefore, it would have been obvious to one having ordinary skill in the art to use transistor as a switch between Miyanaga et al.'s pad and diode for the purpose of reversible turning on/off the switch. Thus, the modified Miyanaga et al.'s figure 1 further shows that the integrated circuit further comprises

a transistor in series with the clamp diode, the transistor having a gate couple to receive a control signal.

6. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyanaga et al. (USP 5514893) in view of Verhaege et al. (USP 6529359), Djakovic (USP 6351539), Toyashima (US 20010017755) and Sher (USP 6417721) and Grugett (USP 5767733).

As to claim 24, the modified Miyanaga et al.'s figure 1 shows a first transistor in series with the clamp diode (see the rejection of claim 23), the transistor having a gate coupled to receive a control signal; and a second transistor (4) coupled between the pad and the first supply terminal. The modified Miyanaga et al.'s figure 1 fails to show that the clamp diode is a drain-to-bulk diode of the second transistor. However, Grugett's figure 1 shows that the bulk of transistor is connected it source in order to reduce leakage current. Therefore, it would have been obvious to one having ordinary skill in the art to connect the bulk of Miyanaga et al.'s transistors respectively to their sources for the purpose of reducing leakage current.

As to claim 25, the modified Miyanaga et al.'s figure 1 shows all elements of the claim except for a first and second transistors respectively connected between the bulk of the pullup transistor and its source and drain. However, Gugett's figure 4 and 6 show transistors (94, 96) respectively coupled between the bulk of transistor 90 and its drain and source for the purpose of reducing the resistance of transistor 90, thereby increasing the speed. Therefore, it would have been obvious to one having ordinary skill in the art to employ Gugett's teaching to Miyanaga's pull-up and pull-down transistors (4, 5) for the purpose of increasing the speed.

7. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fugate et al. (USP 6525594) in view of Tyckowski (USP 6359408) and Zhu et al. (USP 5933047).

Fugate et al.'s figure 2 shows an electronic system comprising: an integrated circuit comprising: an output buffer comprising a pull-up transistor (22) coupled between a pad (at Vo) and a first supply voltage; and a switch 32 coupled to the bulk of transistor 22, a hot-socket circuit (34) coupled to the pad and the first supply voltage, wherein the hot-socket circuit provides an output having a first state if a voltage on the pad is higher than the first supply voltage and a second state if the voltage on the pad is lower than the first supply voltage. Figure 2 fails to show a logic circuit coupled to the output of the hot-socket. However, Tyckowski's figure 1 shows a logic circuit 29 coupled to the output of comparator circuit 27 in order to allow or prevent the output of the comparator controlling circuit 30. Therefore, it would have been obvious to one having ordinary skill in the art to add Tyckowski's logic gate 29 to couple to the output of Fugate et al.'s comparator 34 for the purpose of disabling the switching function when not need. It is also seen as an obvious design preference to select the bulk of Fugate's transistor 22 to connect to Vdd when the logic circuit is disable dependent upon a particular environment to ensure optimum performance, see Fugate's figure 1. Fugate et al.'s figure 2 further fails to show the detail of the switch 32. However, Zhu et al.'s figure 4 shows an integrated switch circuit (P3, P4, 102). It would have been obvious to one having ordinary skill in the art to use Zhu et al.'s integrated switch circuit for Fugate et al.'s switch 32 for the purpose of saving space. Thus, the modified Fugate et al.'s figure 2 further shows a first transistor (Zhu's P3) coupled between a bulk of the pull-up transistor and a source of the pullup transistor, and having a gate coupled to receive a control signal (output of 34); and a second transistor (Zhu'P4) coupled between a drain of the pullup transistor and the bulk of the pull-up transistor, and having a gate coupled to receive a complement of the control signal; wherein when the control signal is in a first state, the bulk of the pull-up transistor is coupled to the pad and when the control signal is in a second state, the bulk of the pull-up transistor is couple to the first

supply voltage; and a drain-to-bulk diode of the pull-up transistor clamps a voltage received at the pad.

8. Claims 26, 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyanaga et al. (USP 5514893) in view of Verhaege et al. (USP 6529359), Djakovic (USP 6351539), Fugate et al. (USP 6525594), Tyckowski (USP 6359408) and Zhu et al. (USP 5933047).

As to claim 26, 28 and 29, the combination of Miyanaga et al., Verhaege et al, and Djakovic (USP 6351539) (see the rejection of claim 1) shows all elements of the claim except for a switch circuit coupled to the bulk of the pull-up transistor. However, the combination of Fugate et al., Tyckowski, and Zhu et al. (see the rejection of claim 27) shows a circuit having switch circuit (the modified 32 and 34) coupled to the bulk of pull-up transistor 22 in order to prevent sudden voltage drop at the bulk, thereby reducing output noise. Therefore, it would have been obvious to one having ordinary skill in the art to add the modified Zhu et al.'s switch circuit to Miyanaga et al.'s pull-up transistor 4 for the purpose of reducing output noise.

As to claim 30, the combination of the above references shows that the logic circuit is an AND gate.

As to claim 31, the combination of the above references fails to teach plurality of programmable logic elements. However, it would have been obvious to one having ordinary skill in the art to use the modified Miyanaga et al.'s circuit in a circuit comprising programmable logic elements in order to take advantage of the modified Miyanaga's benefit to the programmable logic elements circuit.

9. Claims 32, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyanaga et al. (USP 5514893) in view of Verhaege et al. (USP 6529359), Djakovic (USP

6351539), Toyashima (US 20010017755), Sher (USP 6417721) and Fugate et al. (USP 6525594).

The combination of Miyanaga et al., Verhaege et al., Djakovic (USP 6351539), Toyashima, and Sher (USP 6417721) references shows all limitations of the claims (see the rejection of claims 23+) except for a well-bias circuit. However, Fugate et al.'s shows a circuit having well-bias circuit (32 and 34) to select to bias highest voltage to transistor's well in order to reducing leakage current. Therefore, it would have been obvious to one having ordinary skill in the art to add Fugate et al.'s well bias circuit to the modified Miyanaga et al.'s figure 1 to control the pull-up transistor and the switch transistor for the purpose of reducing the transistors' leakage current.

Response to Arguments

10. Applicant's arguments have been fully considered but they are not persuasive.

In response to the arguments regarding the rejection of claim 1, a new ground rejection is introduced as necessitated by amendment. Verhaege et al.'s driver has ESD protection circuit. Thus, circuit breakdown will be prevented; thereby operation cost will be less by eliminating parts replacement.

Applicant states similar arguments regarding the rejection of claim 9. Therefore, similar responses are applied.

In response to the arguments regarding the rejection of claim 27, Tyckowski's figure 1 shows that AND gate 29 connected between comparator 27 and circuit 30 to allow/prevent the output of the comparator 27 to reach circuit 30. One skilled in the art would have motivated to add Tyckowski's AND gate between comparator 34 and circuit 32 in order to allow/prevent the output of comparator 34 reaches circuit 32; thereby having more flexibility of controlling the substrate of transistor 22.

Applicant states similar arguments regarding the rejection of claim 32. Therefore, similar responses are applied.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUAN TRA whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/QUAN TRA/
Primary Examiner, Art Unit 2816